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Design of BIST with Low Power Test Pattern Generator

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Abstract: Mixed mode BIST schemes use pseudo-random patterns to detect most faults. Theoretical analysis suggests that significantly more care bits can be encoded in the seed of a Linear Feedback Shift Register (LFSR). In this paper we implement low power BIST for 32-bit Vedic multiplier. Main aspect of this is to implement low power BIST with increased fault coverage. This use the LFSR as test pattern generator with changing the seed values for every 2 power m cycle, so for this purpose which uses the counter for monitoring the number of cycles. The objective of this work is to reduce power dissipation in BIST with increased fault coverage. Various methods of pattern generation are compared keeping in view of power consumption. For this purpose m bit binary counter & gray code generator is used. Signature analysis is done with the help of multiple input Signature Register (MISR). The signature of MISR will indicate whether the circuit under test (CUT) i.e Vedic multiplier is faulty or not. The results are tabulated and compared. From the implementation results, Simulation is carried out in Xilinx ISE and the design is implemented using Vertex 5 Field Programmable Gate Array (FPGA).

Keywords: Vedic multiplier, Test Pattern Generation, MISR, CUT.

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation. The main aim of these devices is to reduce the power dissipation with high fault coverage. Generally power dissipation of a system in test mode is more than in normal mode. Testing of integrated circuits is important to ensure high level of quality in products. The Built-In-Self-Test (BIST) is one of most popular test solutions to test the embedded cores. Test pattern generation is vital in any BIST circuit. Since off-chip communication between the FPGA and a processor is bound to be slower than on chip communication and in order to minimize the time required for adjustment of the parameters, the built in self test approach is proposed for this method.

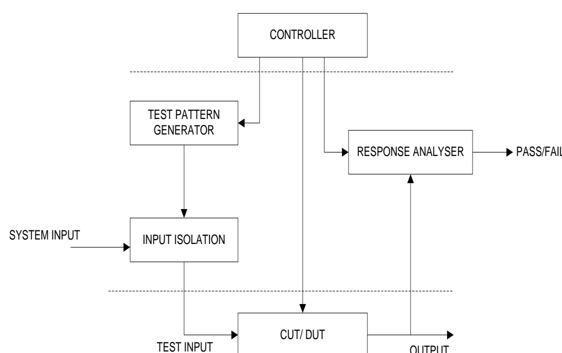

Fig. 1 Block diagram of Built In Self Test

The generic BIST is shown in Fig. 1. BIST solution consists of several blocks given below. a) Circuit under test (CUT) : It is the portion of the circuit tested in BIST mode. It can be combinational, sequential or a memory. b) Test pattern Generator (TPG): This is a circuit to be tested, a way to compress those results & way to analyze them. It generates the test patterns for CUT. Here a Linear feedback shift register is used to generate patterns. Patterns are generated in pseudo random fashion. c) Test controller: It controls the test execution. It provides the control signal to activate all blocks. If control signal is 0, then BIST is said to be in test mode & if 1, normal mode. d) Response Analyzer: It acts as a comparator with stored responses. Compares the test output with the stored response and shows whether the chip passes or fails the test.

BIST architecture is based on Linear feedback shift register whose input bit is logic function of its previous state. An LFSR basically consists of an interconnection of D-flip-flops, XOR gates, forming a shift register with feedback. Mainly LFSR"s are used for pseudo random generation such as TPG"s, ATPG, code convolution techniques. The initial value of LFSR is called seed value. This seed value is always represented in Galois field format or normal binary format also called characteristic polynomial expression of a unit. The initial value of LFSR should be non zero value i.e any one of the bit should be high. If it is zero value then LFSR will be in zero lock state where it produces only zero value to all the clock pulses. The selection of characteristic polynomial is based on the number of faults to be covered.

Before the overall design is synthesized, the four LFSR based test pattern generations is incorporated into CUT. There are different test pattern generators. They are

A. LFSR Type I
B. LFSR Type II

C. Multiple polynomial
D. Cellular Automaton LFSR

All these circuits are described in Verilog HDL and implemented on Vertex 5 FPGA.

II. CONVENTIONAL METHOD

A.LFSR Type I:

LFSR type I is commonly used TPG and is called External LFSR. It consists of D flip flops and XOR gates. The XOR gates are in external feedback. LFSR can cycle through 2^{n-1} distinct states, all zero state is omitted. LFSR type I is

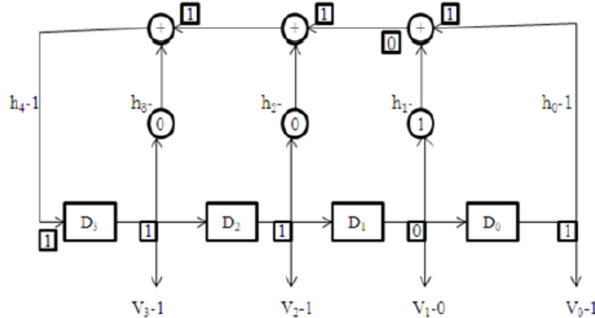

Fig 2: LFSR TYPE 1

B.LFSR Type II:

LFSR type II is called Internal LFSR. It has the linear elements interspersed between flip flops. There are n flip-flops, so it is called an n-stage LFSR. LFSR can cycle through 2^{n-1} distinct states, all zero state is omitted. The main difference between LFSR type I & type II is that in type I the XOR gates are in external feedback and in type II the XOR gates are internal i.e. in between the flip-flops.

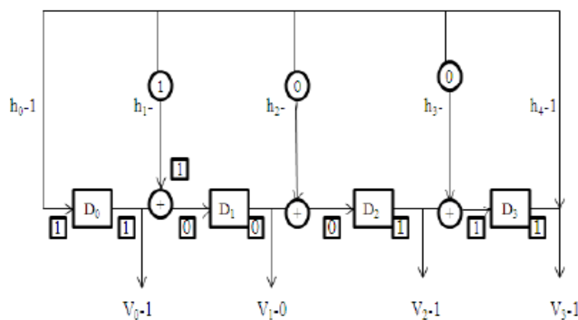

FIG 3: LFSR TYPE 2

III. PROPOSED METHOD

A. Low power Test Pattern Generator:

Here a Linear feedback shift register is used for generating test patterns with reduced switching activities. The LP-TPG consists of m bit counter, gray code generator, LP-LFSR, NOR gate structure and XOR gate.

The m bit counter is initialized with zeros, which generates 2^m test patterns. Counter and gray code generator are synchronized with common clock. When counter output is all zero pattern, NOR gate output is one. Only when the NOR gate output is one, the clock signal is applied to activate the LP-LFSR to generate the next seed. This seed and the output sequence from the gray code generator are exclusive OR to generate the final output. This effectively reduces the switching activities which results in low power. For every 2^m clock cycles the seed value is changed and here no decoding logic is used. Also the selection of polynomial depends on number of faults to be covered which is not the case for other existing methods. So fault coverage is high and high randomness is introduced. The low power test pattern generator is shown in figure 6 in this circuit the power dissipation and power consumption will be less compare to other circuit

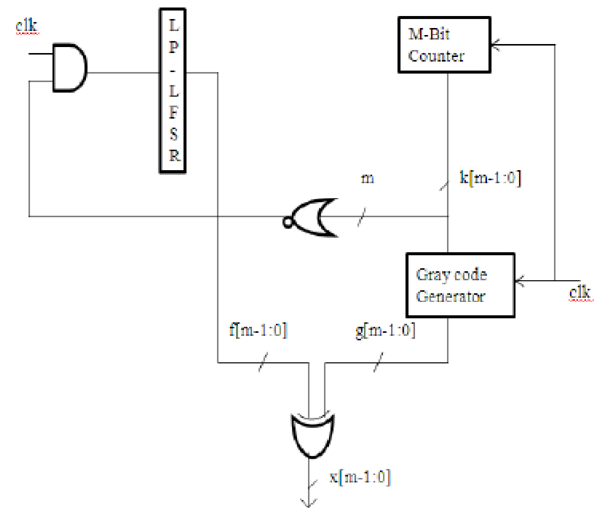

FIG 4: Low Power Test Pattern Generator

E. Vedic Multiplier

After implementing the Low Power Test Pattern Generator The 16-bit Vedic multiplier is used and the test pattern generating seed value is given to the 16 bit Vedic Multiplier

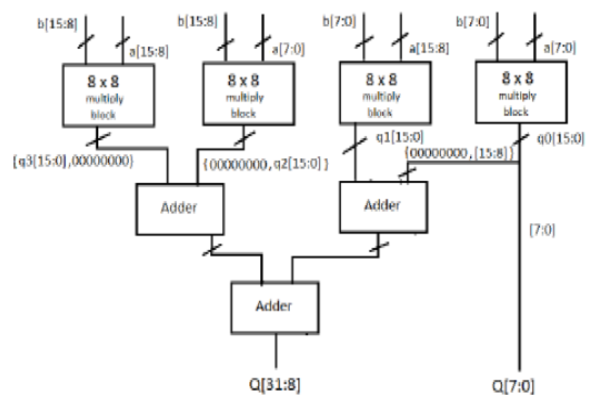

FIG 5: 16x16 Vedic Multiplier

Algorithm for Vedic multiplier: The algorithm for N*N bit Vedic multiplier is given below[6]: Consider for any number of bits in input, let the multiplication of two N-bit binary numbers (where N=1,2,3…N) A and B where A = AN…A3,A2,A1 and B= BN…B3,B2,B1.The final multiplication result will be N+N bits as S=S(N+N)…S3,S2,S1.

Step1: Divide the multiplicand A and multiplier B into two equal parts each consisting of [N to (N/2)+1] bits and [N/2 to 1] bits, respectively where first part represents MSB and other is LSB.

Step2: Now represent parts of A as AM and AL So that A= {AM AL}. B as BM and BL So that B= {BM BL}. **Step3:** Using the Vedic multiplication fundamentals, taking 4 bits at a time and 4 multiplier blocks, multiplication operation is performed. **Step4:** The outputs of [(N/2)*(N/2)] bits are added (i.e 8*8 bits for a 16 bit multiplier) accordingly to obtain the final output. For a 16*16 multiplier, 3 ripple carry adders are used.

A response analyzer is a comparator with stored responses or an LFSR used as signature analyzer. It analyses the value sequence on primary output and compares it with expected output. Signature analysis is done with the help of multiple input signature register (MISR). Here we assume that the CUT has n outputs. It is seen that this circuit operates as n single-input signature analyzers. An n-stage MISR has the property that the parity over all the bits in the input streams equals the parity of the final signature. After 16 clock cycles the seed value is changed. The signature of MISR will indicate whether the circuit under test i.e Vedic multiplier is faulty or not. The polynomial used in the BIST is given as P*(x)= x31+x29+x28+x20+x18+x16+x13+x9+x7+x4+x3+x2 & G(x)=0000000000000101. The input sequence can be represented by the polynomial G(x) and the output sequence by Q(x). The highest degree of polynomials G(x) and Q(x) correspond, respectively, to the first input bit to enter the LFSR and the first output bit produced n clock periods later, and where n is the degree of the LFSR. If the initial state of the LFSR is all) s, let the final state of the LFSR be represented by the polynomial R(x)

IV. SIMULATION RESULTS

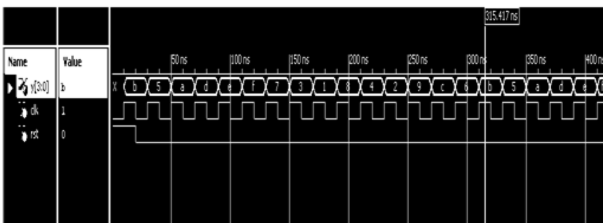

FIG 6: Simulation result of LFSR TYPE 1

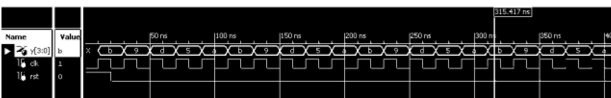

FIG 7: Simulation result of LFSR TYPE 2

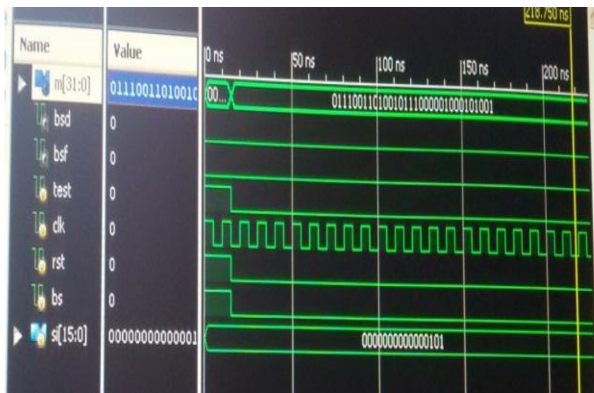

FIG 8: Simulation result of Low Power Test Pattern Generator

V. APPLICATION

1. The BIST is mainly used in the Automotive, Aviation and Integrating circuit manufacturing
2. The BIST is mainly used in the military which was the Minuteman was the first one of the major weapons systems to field a permanently installed

VI. CONCLUSION

In this paper a low power Test Pattern Generator has been incorporated in BIST developed for Vedic multiplier. The switching activities are reduced in the test pattern generation. Fault coverage is increased by the maximum number of clock cycles of the binary counter. The power consumption of different test pattern generation techniques has been found out and compared with the latest method. BIST is implemented for low power test pattern generator i.e. Vedic multiplier in the latest method. It is observed that the power consumption is reduced along with increased fault coverage when compared to other implementations.

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